A Report on

FPGA Design Challenge

Date:	5-04-2025
Time:	9.00AM – 12.00Noon
Venue:	AV Room, ECE Department, SCET
Student coordinators:	Sulaxna Pandey, Tisha Patel
Faculty coordinators:	Prof. Dr. Nehal Shah
Participants:	
Jury / Resource Person	Prof. Dr. Nehal Shah, Ms. Fatema Kotawala
About Event:	A State Level Project Competition on **FPGA Design Challenge** was organized at EC Department, under RnD Cell SCET supported by IETE Surat Center. The FPGA Design Challenge was organized to encourage students to apply their theoretical knowledge in practical hardware design using FPGA technology. The event aimed to foster innovation, problem-solving skills, and hands-on experience with real-world digital design projects. Students enthusiastically participated by designing a variety of projects, showcasing their creativity and technical expertise. During challenge students of ECE showcase their digital design capabilities using state diagrams, programming capabilities using Verilog HDL and hardware demonstration using FPGA boards.
Schedule of Event:	Project Creation & Presentation Project Evaluation & Judging Prize Distribution & Closing **Total Duration:** 3 hours 30 mintues
Key Highlights of the event:	**Diverse Project Range:** Participants presented projects such as Tic Tac Toe game, Microprocessor design, Traffic Light Controller, 8x8 Array Multiplier, Visitor Counter, Automated Car Parking System, among others. **Judging Panel:** An experienced industry expert and academician was invited to evaluate the projects, offering professional insights and constructive feedback.

	Interactive Sessions: The judge engaged with students during the event, providing motivational talks and technical knowledge beyond regular curriculum topics. **Collaborative Environment:** The event fostered peer learning, with students discussing challenges and innovative approaches with each other.
Content Beyond Syllabus:	The challenge encouraged participants to delve into advanced FPGA concepts and real-time applications which are typically not covered in the standard syllabus. Students worked on integrating logic design with system-level thinking, including: ● Implementing complex combinational and sequential circuits. ● Developing real-time embedded systems with FPGA. ● Optimizing design for performance and resource utilization. ● Applying debugging and testing methodologies in FPGA development. This exposure significantly enriched their understanding and skill set, bridging the gap between academic theory and industry practice.
Major Outcome:	• **Enhanced Practical Knowledge:** Students gained hands-on experience in FPGA programming and digital design tools, boosting their technical confidence. • **Problem-Solving Skills:** Encountering real-world design challenges improved analytical thinking and troubleshooting capabilities. • **Feedback for Improvement:** The judge's feedback highlighted areas for growth such as timing optimization, design modularity, and better documentation practices. • **Motivation for Future Projects:** Encouraged by the event, many students expressed interest in pursuing further research and projects in embedded systems and digital design. • **Networking:** The event provided a platform for students to connect with experts and peers, fostering a collaborative learning community.
Participants Feedback:	The students who participated in the FPGA Design Challenge expressed great enthusiasm and appreciation for the event. Many highlighted how the hands-on experience with FPGA projects deepened their understanding of digital design concepts beyond traditional classroom learning. The judge's constructive feedback and motivational insights were especially valued, helping students recognize their strengths and focus on areas for improvement. This guidance inspired participants to enhance their skills and pursue further projects in embedded systems and FPGA design. Moreover, the excitement of competing for the attractive prizes added a healthy competitive spirit, motivating the students to put forth their best efforts. The rewarding experience of showcasing their projects and receiving recognition boosted their confidence and encouraged continued learning and innovation.

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<tr><td></td><td>Overall, the participants described the event as highly motivating, educational, and enjoyable — a perfect blend of challenge, learning, and celebration.</td></tr>
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<tr><td>Winners of the Event:</td><td>
<table>
<tr><th>Winners Name</th><th>Title of Project</th><th>Rank</th></tr>
<tr><td>Arya Kavani, Naninesh Gurav, Aayush Jariwala</td><td>Tic Tac Toe game</td><td>1st</td></tr>
<tr><td>Abhishek Boricha, Bhavya Sondigala, Riddhi Kapadia, Kelvin Sharda</td><td>Design Simple Microprocessor</td><td>2nd</td></tr>
<tr><td>Tathya Shah, Shrey Shah, Deep Vasoya, Deep Ramani</td><td>4-way traffic light control</td><td>3rd</td></tr>
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Sarvajanik College of Engineering and Technology

Electronics & Communication Department

(Re-Accrediated by NBA, New Delhi for 3 years, W.E.F1 July 2022)

FPGA DESIGN CHALLENGE

- State level FPGA design challenge
- Team Size: Max 4
- Combinational/Sequential Circuit
- FPGA/CPLD Board Mandatory
- Resources Provided: Power supply, Digital Trainers
- Win Exciting Prizes
- E-Certificate Provided

REGISTRATION FREE!

Date:
5th April, 2025

Timings:
9:00 to 11:00 AM

Location:
EC Department Labs

Student Coordinator:
Sulaxna Pandey - 7874846095
Tisha Patel - 9023320193

Faculty Coordinator :
Prof. Nehal Shah