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Sarvajani Education Society

Sarvajani College of Engineering & Technology

Dr. R. K. Desai Marg, Opp.Mission Hospital, Athwalines, Surat-395001

Report on

“FPGA Design Challenge 2.0”

In Celebration of National Technology Day

Date: 18th April 2026

Venue: EC AV Room, SCET

Faculty Co-ordinators

Dr. Nehal Shah

In association with

Institution's Innovation Council (IIC), SCET

Introduction

In celebration of National Technology Day which would be on 11th May 2026, we have celebrated and planned this event in the month of April 2026 as May is vacation duration for all stakeholders. The Department of Electronics and Communication Engineering at Sarvajani College of Engineering and Technology successfully organized the “FPGA Design Challenge 2.0” in association with RnD Cell SCET, supported by IETE Surat Center. The event was designed as a team-based technical competition to promote innovation, enhance practical knowledge, and develop problem solving skills among students in the field of FPGA design.

The competition witnessed enthusiastic participation, with teams of up to four members demonstrating their creativity, teamwork, and technical expertise. Overall, the FPGA Design Challenge 2.0 proved to be a successful initiative, encouraging practical learning, teamwork, and technological advancement. Such events organized by SCET continue to prepare students to face real-world engineering challenges and contribute effectively to the field of electronics and communication engineering.



The poster is for the 'FPGA Design Challenge 2.0' event. It features a dark blue background with circuit-like patterns. At the top, there are three logos: Sarvajani College of Engineering and Technology (SU), IETE, and a circular logo with a red flame. Below the logos, the text reads 'Sarvajani College of Engineering and Technology, Surat' and 'Electronics and Communication Engineering Department'. A note in parentheses states '(Re-Accredited by NBA, New Delhi for 3 years, W.E.F 1 July 2022)'. The main title 'FPGA DESIGN CHALLENGE 2.0' is prominently displayed in yellow and white, with a gear icon to the right. Below the title, a 'HIGHLIGHTS' section lists: 'Team-based FPGA Design Competition', 'Max 4 students/ Team', 'Win Exciting Prizes', and 'Networking with Tech Enthusiasts'. The 'FACULTY COORDINATOR' is Prof. (DR.) Nehal Shah, and the 'HEAD OF DEPARTMENT' is Prof. (DR.) Chirag Paunwala. The 'STUDENT COORDINATOR' is Parimal Viradiya (99255 26006) and Dharmi Zazadiya (99988 40650). A 'FREE REGISTRATION' section includes a QR code. The event date is '18th APRIL, 2026', the time is '09:00 AM - 11:00 AM', and the venue is 'EC AV ROOM'.

Sarvajani College of Engineering and Technology, Surat
Electronics and Communication Engineering Department
(Re-Accredited by NBA, New Delhi for 3 years, W.E.F 1 July 2022)

FPGA DESIGN CHALLENGE 2.0

HIGHLIGHTS

- Team-based FPGA Design Competition
- Max 4 students/ Team
- Win Exciting Prizes
- Networking with Tech Enthusiasts

FACULTY COORDINATOR: **FREE REGISTRATION**
Prof. (DR.) Nehal Shah

HEAD OF DEPARTMENT:
PROF. (DR.) CHIRAG PAUNWALA

STUDENT COORDINATOR:
Parimal Viradiya
(99255 26006)
Dharmi Zazadiya
(99988 40650)

18th APRIL, 2026
TIME: 09:00 AM - 11:00 AM
VENUE: EC AV ROOM

About Design Challenge:

The program commenced at 9:00 AM in the EC AV Room with the introduction of the esteemed jury members, followed by their warm welcome and felicitation as a token of appreciation. After the opening ceremony, the competition officially began, where participating teams presented their FPGA-based projects in front of the jury panel.

The jury members evaluated each project based on design efficiency, innovation, and practical implementation. They actively interacted with the participants, offering valuable insights, constructive feedback, and technical guidance to help improve their understanding and project outcomes.

The challenge encouraged participants to delve into advanced FPGA concepts and real-time applications which are typically not covered in the standard syllabus. Students worked on integrating logic design with system-level thinking, including:

- Implementing complex combinational and sequential circuits.
- Developing real-time embedded systems with FPGA.
- Optimizing design for performance and resource utilization.
- Applying debugging and testing methodologies in FPGA development.

This exposure significantly enriched their understanding and skill set, bridging the gap between academic theory and industry practice.

Participation Details:

Participation was allowed only in groups

Each group consisted of a maximum of four students

A poster presentation was mandatory, including:

Group details

Block diagram

Brief explanation

Technical specifications and applications

Total 22 teams are registered, A total of 78 students participated in the event.

Event Highlights:

Inauguration Ceremony:

The event commenced with a formal inauguration in the presence of faculty members, coordinators, jury members, and participating students. The organizers highlighted the importance of FPGA in modern engineering applications and its role in Industry 4.0, smart systems, and sustainable development.

Keynote Address by Jury:

Dr. Nehal Shah and **Dr. Vandana Shah** delivered an insightful keynote address emphasizing the **importance of IoT and its diverse applications** across domains such as healthcare, smart cities, agriculture, automation, and environmental monitoring. They also guided students on:

- Enhancing project innovation
- Improving design methodology
- Aligning projects with real-world applications
- Identifying scope for future improvements and commercialization

The address motivated students to think beyond academic requirements and focus on practical implementation and societal impact.

Interactive Session

Prof. Dr. Nehal Shah, Prof. Rahul Gonawala, HoD and Asst. Professor, BMCET, Surat. Shri Devang Kabutarwala, Shri Deepak Sharda, ASIC & Micro arch@Vicharak, Shri Shail Parmar, Building SBCs @Vicharak. These all dignitaries were there for the interaction and evaluation of the student's Demo. Thus, interactive session was conducted between the **jury members and participating students**, where each group received constructive feedback. The discussion focused on:

- Scope for improvement
- Technical feasibility
- Design optimization
- Future development possibilities

This interaction helped students gain valuable insights into project refinement, research orientation, and professional presentation skills.







Conclusion:

This challenge enhanced practical understanding of FPGA design concepts through hands-on project development.

- Improved problem-solving and analytical skills by working on real-world technical challenges.
- Strengthened teamwork and collaboration among participants in a competitive environment.
- Gained valuable technical feedback and guidance from expert jury members.
- Increased confidence in presenting technical ideas and projects effectively.
- Exposure to innovative design approaches and diverse project ideas.
