Sarvajanik Education Society

Sarvajanik College of Engineering and Technology, Surat

A constituent college of Sarvajanik University

AICTE Training and Learning (ATAL) Academy SPONSORED

One Week Faculty Development Program

On

Silicon Chip Design from Circuits to System, 18th Dec – 23rd Dec 2023

Report

AICTE ATAL sponsored one-week Faculty Development Program (FDP) entitled "Silicon Chip Design from Circuits to System designed by the Electronics and Communication Engineering Department of Sarvajanik College of Engineering and Technology (SCET), a distinguished constituent of Sarvajanik University was organized from December 18th to December 23rd, 2023. Program was designed in line with objective of ATAL (AICTE training and learning academy) for supporting technical institutions in fostering research, innovation and entrepreneurship through training in emerging area of Semiconductor design and development.

At the time of designing FDP, all the aspects of chip design starting from Design cycle, FPGA and ASIC, Physical design, Testing and Verification as well as Analog and RF were incorporated. From system perspective reconfigurable computing, Multicore architectures and System on Chip etc. were included. The aim of FDP was to unravel the intricate pathways of silicon chip design, guiding participants through a transformative journey from fundamental circuits to complex systems.

Inauguration on 18/12/2023

Faculty development program was inaugurated on 18/12/2023 at 9.00AM at Audio Visual Room. National Electronics policy is positioning India as a global hub for Electronics design and manufacturing. Renowned speaker and domain expert, Shri Sudhirbhai Naik, Founder eInfochips Ahmedabad and Chairman, IESA (India Electronics and Semiconductor Association), Gujarat Chapter, were invited as chief guest of the function. Chairman of Sarvajanik Education Society, and Shri Bharatbhai Shah and Prof Persi Engineer, Provost, Sarvajanik University were present and grace the occasion. Shri Sudhirbhai Naik, enlighten all the participants with a roadmap from "**Sand to silicon and impact on global GDP**" during his keynote address.

Day 1 - 18/12/2023

After Inauguration, session was continued with talk on "**Advances in chip development technology"** by Er. Nilesh Ranpura, Director (Engineering), Arrow Inc. (einfochips), Ahmedabad.

During post lunch session, Dr. Kuruvilla Varghese, Chief Research Scientist, Department of Electronic Systems Engineering, IISc Bangalore talked on **"Reconfigurable Computing"** and explained participants, hardware design cannot be done just by reading books or using formulas. He talked about pros and cons of ASIC design and FPGA based design as well as discussed available options of FPGA for various designs. Last session was practical session on **"FPGA and ASIC design cycle"** conducted by Dr. Nehal Shah. In the session, participants were explained to work for front end RTL design in Vivado Tool. After getting exposure to flow, participants were able to test circuits like adder subtractor with mode control, ALU, decoder etc. They were explained to implement Multiplexer with structural, behavioral and dataflow modeling in which various constructs and conditional operator was used.

Day 2 – 19/12/2023

AIML is buzzing word, changing all aspects of our life and similarly EDA tools and chip design technology. Day 2 started with talk entitled "**AI/ML in EDA Tools for chip design**" by Er. Kamlesh singh Dodiya, from Synopsys, Bangalore. He explained usage of EDA tools in VLSI design and importance of Library and IP utilization. With example he discussed, process is iterative and explained how use of AI/ML in EDA tools optimize process and improve accuracy of design. During journey of data from input to output it is converted from serial to parallel and parallel to serial frequently. Serializer and Deserializer are part of System on chip and were discussed by Er. Ankuj Keshwani from Intel, Bangalore during his session entitled "**SerDes Roadmap and its role in future SoC Design**". He discussed the integration of diverse components into a single chip and the importance of efficient interconnectivity between these components. This involves designing a cohesive system that maximizes communication bandwidth while minimizing latency. Last session was practical session which was continuation of Day 1 practical session on FPGA based design by Dr. Nehal Shah. During session participants explored sequential circuits and FSM (finite state machine) based design.

Day 3 – 20/12/2023

On the third day, Er. Prananv Vyas, Associate Director – RTLtoGDS, Arrow Inc. (einfochips), Ahmedabad, started his session on "**Physical Design – A case study**". He talked about various stages of Physical design and role of Engineer at various stages. In the second half Er. Moksh Sancheti from eInfochips talked about Testing ASICs in his talk entitled "**ASIC faults and DFT for complex ASICs**". He explained types of faults and how the test patterns are generated for a different type of fault. Second session was conducted by Dr. Gopal Agarwal, Assistant Professor, IIIT Surat on "**Low dropout voltage regulator"** which was followed by **"Special Airport Systems - An airport case study for Telecom System Design"** by Er. Priyank Trivedi, Assistant Sr. Engineer Jacobs Navi Mumbai. Dr. Gopal has shown demonstration of design of regulator using spice simulation.

Day 4 – 21/12/2023

On the fourth day, there was session on **"Algorithms and architectures"** by Dr. Anand Darji, Professor from SVNIT Surat. In post lunch session, Er. Avi Patel, Co-Founder & Director at Green IP Core, Ahmedabad, talked on **"Selection of Intellectual property core**" for the system design. He demonstrated that signal generated by electromagnetic pulse generator disrupt function of circuit which was implemented on FPGA. After demonstrating many faults he also demonstrated that their own IP core design which is made to overcome such faults can protect chip from such noise. He gave inspiration to participants for converting their ideas into IP core. Practical session was conducted on "**Schematic and Layout**" by Dr. Nehal Shah.

Day 5 – 22/12/2023

On the fifth day, industrial visit was planned to Sahjanand Technologies private limited (STPL). All the participants assemble at SCET by 9.00AM and proceed towards STPL. After reaching at STPL, there was process of registration and followed by presentation from company associates. In presentation they explained about how STPL started various businesses and currently on which technology they are working. After presentation, they showcase various types of 3D machines and how machines are working. Many 3D printed models were shown. Er. Munjal Gajjar, VP - R & D, STPL explained process and technology behind diamond cutting. They also demonstrated how raw stone is analyzed and marked so that maximum size of diamond can be achieved. There was another laser cutting machine which can cut the marked diamond. One more machine was demonstrated which can take diamonds on conveyor belt and cut as per need. Before that diamond is tagged and machine can identify dimension from tag. The whole process was automated. Subsequent sessions was on **"Multicore Processor Architectures**" and "**Tools and Technology for Multicore Processors**" were conducted by Er. Akshay Joshi, CEO at PicusTech Software, Surat and Dr. Harikrishna Parmar, Sr. Software Engg., PicusTech Software, Surat. Topics covered included multicore processor basics, architecture, parallel processing, resource sharing, scalability, OpenMP, MPI, CUDA, OpenCL, thread libraries, parallelism, concurrency, load balancing, and scalability. Dr. Harikrishna Parmar also provided hands on session to the participants.

Day 6 – 23/12/2023

Most of Electronics devices are wireless today, which is only possible due to radio frequency. Dr. Venumadhav Bagvatulla from Samsung Electronics talked about **"Advances in Radio frequency ICs"** He covered 2G and 3G mobile circuits design issues with calculation. He also narrated importance of each block in transmitter and receiver and challenges in their design.

Every day one hour was provided for Article discussion during which in group of 5-6 members, participants discussed given journal papers and summarized key principles and practices from those articles. On the last day time was given to prepare reflective journals stating major outcomes of the FDP as well as concepts or ideas they like to implement. All participants submitted summary of Journal articles and reflective journal after that test was conducted using

Google forms. After completing all submissions, participants were given time to provide feedback on ATAL portal. In addition to feedback on ATAL portal, every day Google form were shared after each session and feedback were collected. At the end interactive session was arranged with all the participants in which they shared their learning experience and verbal feedback.

To summarize, this FDP introduced the journey from Verilog code to circuit, chip and system design with IP cores and EDA tools. With variety of sessions it included the glimpse of current developing techniques, latest technology and future trends in the field from CMOS, FPGA, ASIC, FinFET etc. It also covered digital, Analog and Radio frequency domain from simple to complex SoC. With this overall structure of FDP, time spent at SCET was fruitful for all the participants and their technical knowledge was elevated.

Dr. Nehal N Shah
Coordinator

Dr. Maulin M Joshi
Co-coordinator

Encl.
Photographs of various sessions

Inauguration session


Key Note Address by Er. Sudhir Naik

Session by expert Mr. Nilesh Ranpura


Session by expert Dr. Kuruvilla Varghese

Session by expert Er. Kamlesh Singh Dodiya

Session by expert Er. Ankuj Keshwani


Session by expert Er. Pranav Vyas

Session by expert Er. Moksh Sancheti

Session by expert Dr. Gopal Agarwal

Session by expert Er. Priyank Trivedi

Session by expert Dr. Dr. Anand Darji

Session by expert Er. Avi Patel

Session by expert Er. Akshay Joshi

Session by expert Dr. Harikrishna Parmar

Session by expert Dr. Venumadhav Bhagavatula

Session by expert Dr. Nehal N Shah

Group Photo Day 2

Group Photo Day 3

Group Photo @STPL Industrial Visit

Group Photo Day 6