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SARVAJANIK UNIVERSITY
Sarvajanik College of Engineering and Technology
Bachelor of Technology

Year: B. Tech II (Semester III)

Subject Name: Computer Organization and Architecture **Subject Code:** BTCO13302
Type of course: Professional Core Course
Prerequisite (if any): Basic Electronics

Rationale: With this course, the students will get exposure to fundamental components of the digital systems, as well as combinational/sequential digital circuits. Students will get knowledge of application of digital circuits in architecture and organization of a computer system. The course will include the concepts of different arithmetic-logic-shift operations and their corresponding micro-operations performed by digital computer systems. The importance of pipeline to improve the performance of digital computer is also covered in the course.

Teaching and Examination Scheme:

Teaching Scheme				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	
3	0	2	4	60	25	15	30	20	150

CA1: Continuous Assessment (assignments/projects/open book tests/closed book tests) CA2: Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems TEE: Term End Examination TEP: Term End Practical Exam (Performance and viva on practical skills learned in course) CA3: Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

Content:

Sr. No.	Contents	Total Hours
1.	**Introduction:** **Number Systems** – Various number systems (Decimal, Binary, Octal, Hexadecimal) and conversion between them, Binary Addition, Subtraction, Multiplication, Division, Representation of Signed numbers and binary arithmetic in computers, Various Binary Codes. **Logic Gates** – Introduction, different logic gates (AND, OR, NOT), Universal gates (NAND, NOR), EX-OR, EX-NOR **Boolean Algebra** – Introduction, Laws of Boolean Algebra, Boolean Expression, Reducing Boolean Expression, SOP and POS forms, Karnaugh map -Simple and Multivariable K-map, Don't care conditions	08
2.	**Combinational Circuit :** Half Adder, Full Adder, Half Subtractor, Full Subtractor, Binary Parallel Adder, Encoder, Decoder, Multiplexer, Demultiplexer	05

3.	**Sequential Circuits :** **Flip-Flops** - Basic Concepts of Sequential Circuits; Flip-flops, Triggering of flip-flops, Analysis of clocked sequential circuits, Flip-flop excitation tables, **Registers** – Introduction to shift registers, data transmission in shift registers **Counters** - Introduction to counters, Asynchronous counters, Ripple up-down	07
4.	**Basic Computer Organization and Central Processing Unit :** **Computer Organization and Design** - Instruction codes, Computer registers, Basic computer instructions and its format, Timing and Control, Memory-Reference & Input-output & Register Reference Instructions, Instruction cycle, Interrupt and Interrupt Cycle, Complete computer description, **Central Processing Unit(CPU)** – General Register Organization, Stack Organization, Instruction format with Addressing Modes, Data transfer and manipulation, Program control, Program Interrupt, Types of interrupt, Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC)	11
5.	**Computer Arithmetic:** Data representation in IEEE format, Addition and subtraction, Multiplication Algorithms (Booth Multiplication Algorithm), Division Algorithms, Floating Point Arithmetic operations, Decimal Arithmetic Unit.	05
6.	**Pipeline :** Introduction to parallel processing and pipeline- Flynn's Taxonomy, Instruction Pipeline, Arithmetic Pipeline	05
7.	**Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory	04

Suggested Specification table with Marks (Theory): (For B.Tech only)

Distribution of Theory Marks					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
10	20	15	15	-	-

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

Sr No	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
1	Fundamentals of Digital Circuits	A. Kumar	Prentice Hall India	2016	4th Edition

			ISBN: 8120352688		
2	Computer System Architecture	M. Morris Mano	Pearson Education ISBN: 9789332585607	2017	3rd Edition
3	Digital Fundamentals	Floyed Thomas L. and Jain R. P.	Pearson Education ISBN: 1292075988		11th Edition

Course Outcomes:

Sr. No.	CO statements	Marks % weightage
CO-1	Understand the structure of various number systems and their application in digital system design	15%
CO-2	Design and analyze combinational and sequential logic circuits	20%
CO-3	Identify and explain various instructions and their corresponding microoperations.	15%
CO-4	Design processing unit using the concepts of ALU and control logic	20%
CO-5	Solve various arithmetic algorithms for several data representations	15%
CO-6	Describe fundamentals concepts of pipeline and memory mapping techniques	15%

List of Open learning website:

1. NPTEL : https://nptel.ac.in/courses/117/105/117105080/
2. Udemy : https://www.udemy.com/course/electronics-digital-circuit-design/
3. Coursera : https://www.coursera.org/learn/digital-systems
4. IIT Bombay virtual laboratory: http://vlabs.iitb.ac.in/vlab/

List of Open Source Software:

1. Logisim
2. Logic Circuit Simulation Pro
3. https://logic.ly/demo
4. https://circuitverse.org/
5. https://simulator.io/board

6. BOOLR
7. Xcircuit

For Lab Sessions:

List of Experiments:

Sr. No	Practical
1	Study digital ICs of logic gates - AND, OR, NOT, NAND, NOR, EX-OR and verify their truth tables.
2	Implement different logic gates and verify their truth table using NAND and NOR universal gates.
3	Implement and verify Binary to Gray and Gray to Binary code conversion.
4	Study and configure the following digital circuits (i) Half Adder, (ii) Half Subtractor, (iii) Full Adder, (iv) Full Subtractor
5	Study and configure the following digital circuits (i) Encoder, (ii) Decoder, (iii) Multiplexer, (iv) Demultiplexer
6	Study digital ICs of different flip flops and verify their truth tables.
7	Design 3-bit synchronous up /down counter using digital IC.
8	Design 3-bit Asynchronous up /down counter using digital IC.
9	Study Logisim simulator and verify truth tables for gates – AND, OR, NOT, NAND, NOR, EX-OR. Also design the following combinational circuits using Logisim (i) All Gates Simulations, (ii) Half Adder, (iii) Half Subtractor, (iii) Full Adder, (iv) Full Subtractor
10	Design and simulate the following combinational circuits (i) 2 x 1 Mux, (ii) 1 X 2 Demux, (iii) 8 x 1 using two 4 x 1
11	Design and simulate the following arithmetic circuits (i) 4-bit Binary Adder, (ii) 4-bit Binary Subtractor, (iii) 4-bit Binary Mode Adder/Subtractor
12	Design and simulate the following Sequential circuits

	(i) Explore all the flipflops, (ii) 4-bit asynchronous up/down counter (iii) 4-bit synchronous up/down counter, (iv) n-bit ring counter
13	Design and simulate following memory components. (i) Explore RAM, ROM and TTY Design in Logisim, (ii) Design memory interface for 1024 x 7 RAM memory using 256 x 7 RAM memory.
14	Design the following common bus system using MUX and controlled buffer (i) 2-bit per register, (ii) 4-bit per register
15	Design and simulate the one stage ALU with the following circuits (i) 4-bit arithmetic circuit, (ii) 4-bit logic circuit, (iii) One stage of arithmetic and logic circuit using combination of the above two sub-circuits

Major Equipment Needed:

1. Digital Trainer Kit
2. BreadBoard, connectors
3. IC's of Gates, Flip Flops, Decoders, MUXs, Encoders