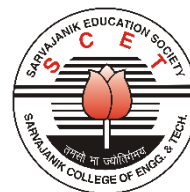




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**Sarvajanik College of Engineering and Technology**  
**Bachelor of Technology**



**B. Tech. Semester III**

**Subject Name:** Digital System Design

**Subject Code:** BTEC13302

**Type of course:** PCC

**Prerequisite:** Basic Electronics and Number Systems

**Rationale:** The students need to learn basic concepts of digital circuits and systems which leads to the design of complex digital systems such as microprocessors. The students need to know combinational and sequential circuits using digital logic fundamentals. The students will learn the design of combinational and sequential circuits. This is the first course by which students get exposure to the digital electronics world.

**Teaching and Examination Scheme:**

Teaching Scheme				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	150
4	0	2	5	60	25	15	30	20	

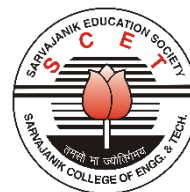
**CA1:** Continuous Assessment (assignments/projects/open book tests/closed book tests) **CA2:** Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems **TEE:** Term End Examination **TEP:** Term End Practical Exam (Performance and viva on practical skills learned in course) **CA3:** Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

**Content:**

Sr. No.	Topics	Teaching Hrs.	Module % Weightage
1.	<b>Introduction:</b> Introduction to number systems and codes, logic gates, Boolean algebra - postulates and theorems, SOP & POS forms, canonical and standard forms, logic minimization using Karnaugh Map, Realizing logic functions using gates.	7	10
2.	<b>Combinational Logic Circuit Design:</b> half adder full adder, BCD adder, code converters, magnitude comparator, multiplexers and decoders, encoder, MSI digital circuit design problems.	8	20
3.	<b>Sequential Logic Circuit Design:</b> Latches and Flip Flops, SR, JK, T, D, and master-slave Flip Flops, Ripple and Synchronous counters, Shift registers, Sequence generators.	10	15
4.	<b>Introduction to Finite State Machines (FSM):</b> Capabilities and Limitations of finite state machines,	8	15



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	Mathematical representation, State transition, State table, MOORE model, MEALY model, Basic concepts in state machine analysis.		
5.	<b>Design of Synchronous and Asynchronous Sequential Circuits:</b> Synchronous circuit Model selection, number of state flip-flops, input forming logic, output forming logic, Design equation and circuit diagram, Algorithmic state machines, Analysis and design of the asynchronous circuit, Applications of State machine.	8	15
6.	<b>Memory and Programmable Logic Devices:</b> Types of memory, Introduction to Programmable Logic Devices, Read-Only Memory, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Complex Programmable Logic Devices (CPLDs), Field Programmable Gate Array (FPGA).	5	10
7.	<b>A to D Converter and D to A Converter:</b> Introduction, Digital to Analog Converter: Weighted Resistor D/A Converter, R-2R Ladder D/A Converter, Specifications for D/A Converters, Sample and Hold, Analog to Digital Converters: Quantization and Encoding, Parallel Comparator A/D Converter, Counting A/D Converter, Dual Slope A/D Converter, A/D Converter Using Voltage to frequency conversation, A/D Converter Using Voltage to time conversation.	5	5
8.	<b>VLSI Design Flow:</b> Design entry: Schematic, FSM & HDL, different modeling styles in Verilog: Behavioral and Structural Modeling, Data types and objects, Synthesis and Simulation Verilog constructs and codes for combinational and sequential circuits.	9	10

**Suggested Specification table with Marks (Theory/Practical):**

% Distribution of Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10	20	20	20	20	10

**Legends:** R: Remembrance, U: Understanding; A: Application, N: Analyze, E: Evaluate C: Create and above Levels (**Revised Bloom's Taxonomy**)

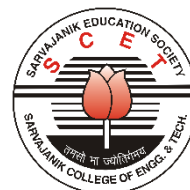
**Note:** This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

**Reference Text Books:**

Sr. No.	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
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1.	Fundamentals of Digital Circuits	Anand Kumar	PHI 988120350526	2014	3 <sup>rd</sup>
2.	Digital Logic and Computer Design	M. Morris Mano	PHI	2018	4 <sup>th</sup>
3.	Modern Digital Electronics	R P Jain	TMH	2010	4 <sup>th</sup>
4.	Digital Principles and Applications	Donald P Leach Albert Paul Malvino Goutam Saha	TMH 9780070141704	2011	7 <sup>th</sup> Indian edition
5.	Digital Logic & State Machine Design	David J. Comer	Oxford University Press	2018	3 <sup>rd</sup> Indian edition
6.	Digital Design	M. Morris Mano and Michael D.	Pearson	2018	6 <sup>th</sup>
7.	A Verilog HDL Primer	J. Bhaskar	BS Publication	2015	3 <sup>rd</sup>
8.	Fundamentals of Digital Logic with Verilog Design	Brown and Vrenesic	Mc Graw Hil	2017	2 <sup>nd</sup>

**Course Outcome:**

Sr. No.	CO statement After learning this subject, students will be able to,	Marks % weightage
CO-1	Apply the knowledge of digital number systems, Boolean algebra, and logic gates for logic function minimization.	25
CO-2	Design and analyze combinational and sequential circuits.	30
CO-3	Design synchronous and asynchronous circuits with state diagram and FSM.	20
CO-4	Comprehend the digital logic families and PLDs.	10
CO-5	Implement digital circuits using Verilog based VLSI design flow.	15

**Mapping with POs:**

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1	3	3	3	2	3	3	1	1	1	1	1	1	2	0	2
CO-2	2	3	2	2	2	1	1	1	2	1	1	1	2	0	2
CO-3	3	3	3	2	3	3	1	2	3	1	1	2	2	2	3
CO-4	1	1	2	1	2	1	1	1	1	1	1	1	2	1	2
CO-5	3	2	3	3	3	3	1	1	3	1	1	2	2	3	3



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**List of practical:**

1. Design and implement half adder, half subtractor, full adder, full subtractor circuit using logic gates. Also implement full adder and full subtractor using control input.
2. To implement all basic gates (AND, OR, NOT, Ex-OR) with the help of the universal gates (NAND, NOR)
3. Design and implement BCD adder using binary parallel adder IC (7483).
4. Implement a clocked JK-Flip Flop using NAND gates. Verify functionality of JK, D, and T flip flop using IC 7474, and 74107 ICs
5. Study of Multiplexer (4:1 IC 74153). Design and implement 8x1 MUX using dual 4x1 MUX.
6. Design and implement  $\sum m(1,2,5,6,7,9,10,15)$  using MUX. Take A, C and D as your select variables.
7. Study Decoder through IC 74138/74154 and Implement full adder using decoder.
8. Use J-K Flip flops & gates. Design 3 bit Synchronous Binary Up counter, Binary Down counter and Binary Up-Down Counter with mode control.
9. Design and implement MOD 5 Synchronous counter.
10. Design and implement 3 bit binary Asynchronous (Ripple) Counter using J-K flip flops.
11. Design and implement BCD ripple counter.
12. Design and Implement the counter for the given sequence (0-3-7-8-A-C-F)
13. Design and Implement shift register using 4-Flip-Flops.
14. Write Verilog code to perform 8-bit ALU and demonstrate on FPGA.
15. Mini Project (Active Learning Assignments)

**Major Equipment:**

- Digital Integrated Circuits Tester, Complete Bread Board Systems with switches and I/O indicators, multimeters, square wave generators, Digital ICs of TTL Logic family, CPLD / FPGA board

**List of Open Source/learning website:**

- <https://nptel.ac.in/courses/117/106/117106114/>  
Digital circuits and System syllabus
- <https://www.youtube.com/playlist?list=PL2140D6A6E9875994>  
Digital circuits and System syllabus

**List of Open Sources of software:**

- [Logisim](#), [Web packages for HDL](#), [Free HDL](#)