SARVAJANIK UNIVERSITY
Sarvajanik College of Engineering and Technology
Bachelor of Technology

B. Tech. Semester IV

Subject Name: **VLSI Design** **Subject Code: BTEC13404**

Type of course: **PCC**

Prerequisite: Knowledge of Basic Electronics, BJT, MOS, CMOS, and Digital Logic.

This course will provide an opportunity for the students to learn about various topics of VLSI such as MOSFET fabrication, its physics, analysis as well as the design of digital circuits using MOSFET devices. In the laboratory part of this course, students will be given exposure to hardware description language such as Verilog for the automated design of digital circuits. Also, some backend tools like Electric and LTSpice can be used for the schematic design and layout design. This subject is very important for students who would like to pursue their careers in the VLSI domain.

Teaching and Examination Scheme:

Teaching Scheme				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	150
3	0	2	4	60	25	15	30	20	

CA1: Continuous Assessment (assignments/projects/open book tests/closed book tests **CA2:** Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems **TEE:** Term End Examination **TEP:** Term End Practical Exam (Performance and viva on practical skills learned in course) **CA3:** Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

Content:

Sr. no.	Topics	Teaching Hrs.	Module % Weightage
1.	**Introduction of Logic family and VLSI Basics:** Overview of logic family, Comparison of RTL, TTL and CMOS logic family, Static, dynamic and short circuit power dissipations, Propagation delay, Power delay product, Fan in, fan out and dependencies Overview of VLSI design methodology and tools, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, computer-aided design technology. Design methodology and tools, Structured design techniques, Types of ASICs, Full-Custom ASICs, Standard-Cell-Based ASICs, Gate-Array-Based ASICs	5	10
2.	**MOSFET Transistor Theory:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET	5	10

	scaling, MOSFET capacitances MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model.		
3.	**Layout and Fabrication:** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design. Parasitic; Technology scaling; Lambda parameter, wiring parasitic, SPICE Models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. Stick Diagrams.	4	15
4.	**MOS Inverters: Static Characteristics:** DC transfer characteristic and Noise margin, Resistive load Inverter, Inverter with n-type MOSFET load Enhancement and Depletion type MOSFET load, CMOS Inverter,	4	10
5.	**CMOS Circuit characterization and performance Estimation:** Delay Estimation: RC Delay Models, Elmore delay model Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Power dissipation in CMOS gates, Static and Dynamic dissipation, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin .	8	15
6.	**Combinational MOS logic families:** Static CMOS Logic: Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and FlipFlops, Design calculations for combinational logic and active area on-chip; Hazards, sources and mitigation techniques, case study; Meta-stability and solutions; Transmission gate, utility, and limitations.	5	10
7.	**Sequential Logic families:** Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop, On-chip Clock Generation and Distribution, Latch-Up and its Prevention.	5	10
8.	**Dynamic Logic families:** Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits, Ratioed Circuits, Cascode Voltage Switch Logic, Domino logic, NORA logic.	4	10
9.	**Design for testability:** Introduction, Fault types and models, Controllability, and observability, AdHoc Testable design techniques, Scan–based techniques, built-in SelfTest (BIST) techniques, current	2	5

	monitoring IDDQ test.		
10.	**FinFET Device:** Introduction (Need of FinFET device), structure, Comparison between FinFET and Planar MOSFET (gm, gds, leakage current, DIBL, Subthreshold Slope).	3	5

Suggested Specification table with Marks (Theory/Practical):

% Distribution of Marks					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
25	25	30	10	10	0

Legends: R: Remembrance, **U:** Understanding; **A:** Application, **N:** Analyze, **E:** Evaluate **C:** Create and above Levels **(Revised Bloom's Taxonomy)**

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from the above table.

Reference Text Books:

Sr. No.	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
1.	Principles of CMOS VLSI Design	Neil Weste ,Kamaran Eshraghian	Pearson Education 8178082225	2001	2nd
2.	CMOS Digital Integrated circuits – Analysis and Design	Sung – Mo Kang, Yusuf Leblebici	TaTa McGraw	2001	Latest
3.	Introduction to VLSI Circuits & Systems	John P. Uyemura	John Wiley	2001	Latest
4.	Digital Integrated Circuits: A Design Perspective	M. Rabaey, A. Chandrakasan and B. Nikolic	Pearson (Low Price Edition)	2016	Latest
5.	FinFETs and Other Multigate Transistors	J. P. Colinge	Springer	2010	Latest

Course Outcome:

Sr. No.	CO Statement After learning this subject students will be able to,	Marks % weightage
CO-1	Describe trends in semiconductor technology and how it impacts scaling and performance.	15
CO-2	Explain fabrication steps, MOS structure, and operation.	15

CO-3	Summarize static and switching characteristics of inverters.	25
CO-4	Calculate delay and interconnect parasitic.	15
CO-5	Draw transistor-level sequential and combinational circuits and their stick diagrams as well as layout.	15
CO-6	Simulate digital logic circuits using a hardware description language.	15

Mapping with POs:

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**	**PSO 3**
CO-1	2	2	1	1	3	1	1	1	1	2	2	1	3	3	3
CO-2	2	2	1	1	3	1	1	1	1	2	2	1	1	3	3
CO-3	2	2	1	1	3	1	1	1	1	2	2	1	3	2	3
CO-4	2	2	1	1	3	1	1	1	1	2	2	1	3	3	3
CO-5	1	2	1	1	3	1	1	1	2	2	2	1	3	3	3
CO-6	1	2	1	1	3	1	1	1	2	1	2	1	3	3	3

List of practical:

First Part – Back end study

Take W/L ratio for NMOS 10/2 and PMOS 20/2.
Rise time = Output reaches from 10% to 90% of Maximum value.
Fall time = Output reaches from 90% to 10% of Maximum value.
Propagation Delay = Average (Rise time + Fall time)

1. Draw schematic of the inverter. Perform timing simulation and measure rise time and fall time.
2. Draw schematic of 2 input NAND gate and 2 input NOR gate. Verify the truth table and measure propagation delay.
3. Draw a layout of the inverter and perform a timing simulation. Measure rise time and fall time. Also, measure the area in (µm) of the inverter.
4. Draw schematic and layout of ring oscillator for 5 stages and 9 stages and identify the maximum frequency of oscillation. Also, measure area in (µm).
5. Draw a layout of 2 input NAND and 2 input NOR gate and perform timing simulation. Measure propagation delay and area of NAND as well as NOR gate.

Second Part – Font end study

6. Write VERILOG code for Full adder. Use VERILOG code of full adder as a component. Using Structural Methodology write VERILOG code for 4-bit adder and 8-bit adder. Show output with at least four combinations of input in a single waveform for an 8-bit adder. Implement an 8-bit adder subtractor with mode control using the behavioral method. Measure synthesis delay and resource utilization for 4 bit as well as an 8-bit adder.
7. Write VERILOG code to realize a

A. . 4×1 multiplexer using structural modeling.
B. 8×1 multiplexer using structural modeling.
C. 8×1 multiplexer using dataflow modeling.
D. 4×1 multiplexer using behavioral code using if-else statement.
E. 8×1 multiplexer using behavioral code using a case statement.
F. Use available 4×1 multiplexer and write code for 8×1 using conditional statement.
G. Use available 4×1 multiplexer and write code for 16x1 multiplexer. Measure and compare synthesis delay and resource utilization for all methods

8. Write VERILOG code for
A. 2×4 decoder using structural modeling.
B. 3×8 decoder using structural modeling.
C. 3×8 decoder using dataflow modeling.
D. 3×8 decoder using behavioral code using a case statement.
E. Use available 2×4 or 3×8 decoder and write code for 4×16 decoder. Show output such that all combinations of inputs are visible

9. Study of programmable devices like FPGA and CPLD. 3 Study Basys3 FPGA board with Artix®-7 FPGA from Xilinx and understand the process of downloading bit files on FPGA as well as execution of code using external inputs.

10. Write behavioral VERILOG code for positive edge-triggered D flipflop with asynchronous reset. Extend the same code for the 8-bit register. Write VERILOG code for 4 –a bit up / down counter using behavioral modeling.

11. Write Verilg code to implement and test simple ALU using behavioral modeling having the following specifications.
- Inputs – A, B (8 bit)
- Opcode – Operation Selection (3 bit - 8 operations) – Add, subtract, Complement, AND,OR, XOR, Comparison, Equality Comparison
- Output – R (8 bit)
- CF – carry out the flag, ZF – Zero flag Measure synthesis delay and resource utilization

12. Write VERILOG code to implement a 3-bit or 4-bit sequence detector using FSM.

13. Write VERILOG code for 8×8-bit ROM with predefined data. Demonstrate reading of data with random/sequential address.

Homework

Try following using Verilog HDL and
A. 8 to 3 priority encoder
B. 8-bit parity generator
C. BCD counter
D. 4 bit magnitude comparator
E. Sequential adder for two 8-bit numbers
F. CLA - Carry Look Ahead adder for two 8-bit numbers
G. Multiplier circuit for two 8-bit numbers

Major Equipment:

- Circuit simulator, FPGA/CPLD programming tool, Multimeter, Power supply, function generator, oscilloscope

List of Open Source/learning websites:

- NPTEL Videos
  (provide link and syllabus covering)

List of Open Source software:

- Spice simulator
- Electric software
- Vivado design suite