SARVAJANIK UNIVERSITY
Sarvajanik College of Engineering and Technology
Bachelor of Technology

B. Tech. Semester VIII

Subject Name: **VLSI Physical Design Automation** **Subject Code: BTEC13802**

Type of course: PEC

Prerequisite: Digital fundamentals, VLSI RTL Design , Layout design and Verilog coding

Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design, logic simulation and verification for automation application .This course aims for covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow application for design automation

Teaching and Examination Scheme:

Teaching Scheme				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	100
3	0	0	3	60	25	15	--	--	

CA1: Continuous Assessment (assignments/projects/open book tests/closed book tests **CA2:** Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems **TEE:** Term End Examination **TEP:** Term End Practical Exam (Performance and viva on practical skills learned in course) **CA3:** Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

Content:

Sr. no.	Topics	Teaching Hrs.	Module Weightage
1.	**Introduction:** VLSI Design, The VLSI Design Process, Layout Styles, Difficulties in Physical Design, Definitions and Notation.	4	10
2.	**Circuit Partitioning:** Introduction, Problem Definition, Cost Function and Constraints, Approaches to Partitioning Problem, Other Approaches and Recent Work	6	14
3.	**Floor planning:** Introduction, Problem Definition, Approaches to Floor planning, Other Approaches and Recent Work.	5	12
4.	**Placement:** Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Placement, Other Approaches and Recent Work	6	14
5.	**Grid Routing:** Introduction, Problem Definition, Cost Functions and Constraints, Maze Routing Algorithms, Line Search Algorithms, Other Issues, Other Approaches and Recent Work.	6	14

6.	**Global Routing:** Introduction, Cost Functions and Constraints, Routing Regions, Sequential Global Routing, Integer Programming, Global Routing by Simulated Annealing, Hierarchical Global Routing, Other Approaches and Recent Work.	5	12
7.	**Channel Routing:** Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Channel Routing, Other Approaches and Recent Work.	5	12
8.	**Layout Generation:** Introduction, Layout Generation, Standard-cell Generation, Optimization of Gate-matrix Layout, Programmable Logic Arrays, Other Approaches and Recent Work.	5	12

Suggested Specification table with Marks (Theory/Practical):

% Distribution of Marks					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
10	15	20	20	15	20

Legends: R: Remembrance, **U:** Understanding; **A:** Application, **N:** Analyze, **E:** Evaluate **C:** Create and above Levels **(Revised Bloom's Taxonomy)**

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Text Books:

Sr. No.	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
1.	VLSI Physical Design Automation, Theory and Practice	Sadiq M. Sait and Habib Youssef	world scientific press	2006	Latest
2.	Algorithm for VLSI physical design automation by - by	Sherwani and navneed	Springer /B S Publication	2008.	Latest
3.	Algorithms for VLSI Physical Automation, Third Edition, , 1998.	N. Sherwani	Kluwer	1998	3rd
4.	Algorithms for VLSI Design Automation,	S. H. Gerez	Wiley	1998.	Latest
5.	Digital Logic Testing and Simulation,	A. Micozo,	Wiley	2003	2nd

6.	Iterative Computer Algorithm with Applications in Engineering,	S. M. Sait and H. Yousuf	Wiley/IEEE	2002.	Latest
7.	Computer Aided Optimization of Digital Integrated Circuits	C. Visweswariah and S. Duvall	Wiley	2002.	Latest
8.	Synthesis and Optimization of Digital Circuits	G. De Micheli	Mcgraw-Hill International	1994	Latest

Course Outcome:

Sr. No.	CO Statement After learning this subject students will be able to	Marks % weightage
CO-1	Apply the concept of different constraints, cost functions and optimization.	25
CO-2	Optimize VLSI design using Circuit Partitioning, Floor planning and placement.	25
CO-3	Use different algorithm in design of CAD tools for VLSI Design.	25
CO-4	Explain various styles of routing for optimization of Area.	25

Mapping with POs:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1	3	2	2	2	2	-	-	-	2	-	2	2	-	-	-
CO-2	2	2	2	2	2	2	-	-	2	2	2	2	2	2	2
CO-3	-	2	2	2	2	2	-	-	2	2	2	2	3	2	3
CO-4	2	2	2	1	2	2	2	1	2	2	2	2	3	2	3

List of Open Source/learning website:

- https://nptel.ac.in/courses/106105161- VLSI Physical Design