SARVAJANIK UNIVERSITY
Sarvajanik College of Engineering and Technology
Bachelor of Technology

B. Tech. Semester VI

Subject Name: **Testing and Verification** **Subject Code: BTEC14602**
Type of course: PEC
Prerequisite: Digital fundamentals , RTL Design
Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, and verification concepts**.** This course aims for covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow

Teaching and Examination Scheme:

Teaching Scheme				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	100
2	0	2	3	60	25	15	30	20	

CA1: Continuous Assessment (assignments/projects/open book tests/closed book tests **CA2:** Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems **TEE:** Term End Examination **TEP:** Term End Practical Exam (Performance and viva on practical skills learned in course) **CA3:** Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

Content:

Sr. no.	Topics	Teaching Hrs.	Module % Weightage
1.	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	3	10
2.	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability.	4	10
3.	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation.	4	15
4.	**Test Generation:** Random Test Generation, Designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification, Designing a Simulation-Based ATPG.	4	15

5.	**Built-In Self-Test and Boundary Scan:** BIST Design Rules, Test Pattern Generation, Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement, Digital Boundary Scan.	4	15
6.	**Verification:** Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages.	4	15
7.	**Functional Verification:** Introduction to test bench, Test bench architecture, Types of test benches, case study.	4	20

Suggested Specification table with Marks (Theory/Practical):

% Distribution of Marks					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
10	15	20	20	15	20

Legends: R: Remembrance, **U:** Understanding; **A:** Application, **N:** Analyze, **E:** Evaluate **C:** Create and above Levels **(Revised Bloom's Taxonomy)**

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Text Books:

Sr. No.	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
1.	VLSI Test Principles and Architectures	Wang Wu Wen	Morgan Kaufmann	2006	Latest
2.	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	M. Bushnell V. D. Agrawal	Kluwer Academic	2000	Latest
3.	Digital Systems Testing and Testable Design	M. Abramovici, M. A. Breuer	IEEE press	1990	Latest
4.	Introduction to Formal Hardware Verification	T. Kropf	Springer Verlag,	2000	Latest
5.	System-on-a-Chip Verification-Methodology and Techniques	P. Rashinkar Paterson	Kluwer Academic Publishers	2001	Latest
6.	Writing Test benches, Functional Verification of HDL Models	Janick Bergeron	Springer	2000	Latest

Course Outcome:

Sr. No.	CO Statement After learning this subject students will be able to	Marks % weightage
CO-1	Describe importance of testing during VLSI lifecycle and challenges in testing.	15
CO-2	Explain design rules and scan architectures for testing RTL designs.	25
CO-3	Generate random test patterns to identify faults in combinational and sequential circuits	25
CO-4	Analyze results of build-in self-test and boundary scan.	20
CO-5	Discuss verification plan, characteristics and methods.	15

Mapping with POs:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO-1	3	2	2	3	2	2	3	-	-	-	2	2	2	-	2
CO-2	3	2	3	3	3	2	2	-	3	2	2	2	2	2	2
CO-3	3	3	3	3	3	2	2	-	3	2	3	2	3	3	3
CO-4	3	3	3	3	2	2	2	-	3	2	3	2	3	2	3
CO-5	3	2	2	3	-	-	2	-	3	3	3	2	2	2	2

List of Practical:

1. Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
2. Write a VHDL/Verilog code to realize functioning of control Point Insertion technique.
3. Write VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered muxed-D scan cell.
4. Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell.
5. Write a VHDL/Verilog code to realize functioning of LSSD double latch design
6. Write a VHDL/Verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain
7. Write a VHDL/Verilog code to realize functioning of Fixing bus contention in scan design rules
8. Write a VHDL/Verilog code to realize functioning of Adding a lock-up latch between cross clock-domain scan cells.
9. To develop an exhaustive test bench for lower level combinational designs: 1. Adder and 2. multiplexer. 10 To develop an exhaustive test bench for J-K flip-flop
10. To develop an exhaustive test bench for 4 bit up-down counter.
11. To verify an 8 bit shift register.
12. To prepare a complete test vector set for all possible stuck at faults parity checker where the data word is of 2 bit.

Major Equipment:

- FPGA,CPLD boards

List of Open Source/learning website:

- https://nptel.ac.in/courses/117103125-VLSI Design Verification and test

List of Open Source Software:

- Ngspice
- Vivado (software)