# SARVAJANIK UNIVERSITY
## Sarvajanik College of Engineering and Technology
**Bachelor of Technology**

**B. Tech. Semester VII**

**Subject Name:** **Mixed Signal Design** **Subject Code: BTEC14702**
**Type of course:** PEC
**Prerequisite:** CMOS Analog circuit design
**Rationale:** This course builds the advanced CMOS analog IC design. This course focuses on the concepts of mixed signal VLSI design. The course will give practical aspects of mixed signal VLSI blocks such as comparators, data converters, oscillators and phase locked loop. In summary, the course is designed for considering the needs of the VLSI design industry.

**Teaching and Examination Scheme:**

| Teaching Scheme | | | | Theory Marks | | | Practical Marks | | Total |
|---|---|---|---|---|---|---|---|---|---|
| L | T | P | C | TEE | CA1 | CA2 | TEP | CA3 | 150 |
| 3 | 0 | 2 | 4 | 60 | 25 | 15 | 30 | 20 | |

**CA1:** Continuous Assessment (assignments/projects/open book tests/closed book tests **CA2:** Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems **TEE:** Term End Examination **TEP:** Term End Practical Exam (Performance and viva on practical skills learned in course) **CA3:** Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

**Content:**

| Sr. no. | Topics | Teaching Hrs. | Module % Weightage |
|---|---|---|---|
| 1. | **Data Converter Fundamentals:** Converting Analog Signals to Digital Signals, Sample-and-Hold (S/H) Characteristics, Digital-to-Analog Converter (DAC) Specifications, Analog-to-Digital Converter (ADC) Specifications, Mixed-Signal Layout Issues. | 6 | 15 |
| 2. | **Data Converter Architectures:** DAC Architectures, Resistor String, R-2R Ladder Networks, Cyclic DAC, Pipeline DAC, ADC Architectures, Two-Step Flash ADC, Successive Approximation ADC, Dual-Slope ADC, Pipeline ADC, Op-Amps in Data Converters. | 8 | 20 |
| 3. | **Switched capacitor circuits**: Sampling switches, Switched capacitor amplifiers, Switched capacitor integrators, Switched capacitor common mode feedback. | 6 | 15 |
| 4. | **Feedback Amplifiers:** Feedback Equation, Properties of Negative Feedback on Amplifier Design, Recognizing Feedback Topologies, The Voltage Amp (Series-Shunt Feedback), The Transimpedance | 10 | 20 |

| | | | |
|---|---|---|---|
| | Amp (Shunt-Shunt Feedback), Transconductance Amp (Series-Series Feedback), The Current Amplifier (Shunt-Series Feedback), Stability. | | |
| **5.** | **CMOS filters:** Integrator building blocks, Filtering topologies. | 6 | 15 |
| **6.** | **Oscillators and PLL:** Ring oscillators, LC oscillators, Voltage controlled oscillators, Phase locked loops, Applications of PLL. | 6 | 15 |

**Suggested Specification table with Marks (Theory/Practical):**

| **% Distribution of Marks** | | | | | |
|---|---|---|---|---|---|
| **R Level** | **U Level** | **A Level** | **N Level** | **E Level** | **C Level** |
| 20 | 25 | 25 | 10 | 10 | 10 |

**Legends: R:** Remembrance, **U:** Understanding; **A:** Application, **N:** Analyze, **E:** Evaluate **C:** Create and above Levels **(Revised Bloom's Taxonomy) Note:** This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

**Reference Text Books:**

| **Sr. No.** | **Title of book /article** | **Author(s)** | **Publisher and details like ISBN** | **Year of publication** | **Publication Edition** |
|---|---|---|---|---|---|
| **1.** | CMOS Mixed Signal Circuit Design | R. Jacob Baker | Wiley India IEEE Press | 2008 | Latest |
| **2.** | CMOS Circuit Design Layout and Simulation | R.Jacob Baker | Wiley IEEE press | 2009 | 2nd |
| **3.** | Design of Analog CMOS Integrated Circuits | Behzad Razavi | McGraw Hill | 2016 | 3rd |

**Course Outcome:**

| **Sr. No.** | **CO Statement After learning this subject students will be able to** | **Marks % weightage** |
|---|---|---|
| **CO-1** | Explain analog to digital and digital to analog converters. | 15 |
| **CO-2** | Describe architectures of ADCs and DACs. | 15 |
| **CO-3** | Explain switched capacitor amplifiers, integrators and feedback mechanism. | 20 |
| **CO-4** | Discuss properties of negative feedback amplifiers, filters and oscillators | 20 |
| **CO-5** | Design parameters for various feedback amplifier topologies and filters. | 15 |
| **CO-6** | Apply oscillators and phase locked loops. for various mixed signal design based applications | 15 |

**Mapping with POs:**

| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 | PSO 3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO-1** | 2 | 2 | 2 | 2 | 2 | 2 | - | - | 2 | - | - | 2 | 2 | 2 | 2 |
| **CO-2** | 2 | - | 2 | - | - | - | - | - | - | - | - | 2 | 3 | 2 | 2 |
| **CO-3** | 2 | 2 | 2 | 2 | 2 | 2 | - | - | 2 | - | - | 2 | 2 | 2 | 2 |
| **CO-4** | 1 | - | - | - | - | - | - | - | - | - | - | | 2 | 2 | 2 |
| **CO-5** | 2 | 2 | 2 | 2 | 2 | 2 | - | - | 2 | 2 | 2 | 2 | 2 | 2 | 2 |

**List of Practical:**

1. To obtain ON resistance of following devices when using a switch using simulation: 1. NMOS 2. PMOS 3. Transmission Gate .
2. To obtain the error in sampled voltage when following devices use a switch using simulation: 1. NMOS 2. PMOS 3. Transmission Gate.
3. To study and simulate dummy device based charge injection cancellation technique. Obtain the error in sampled voltage.
4. Simulate switched capacitor amplifier circuit.
5. To simulate basic clock signal based sense amplifier circuit and measure its performance parameters.
6. To simulate and analyze charge pump PLL.
7. To simulate regenerative feedback based CMOS comparator circuit and measure its performance parameters.

**List of Open Source Software:**

- ngspice/multisim (software)