SARVAJANIK UNIVERSITY
Sarvajanik College of Engineering and Technology
Bachelor of Engineering

SARVAJANIK UNIVERSITY
INCLUSIVE | INTEGRATED | INNOVATIVE

B. Tech. Year II Semester – 3

Subject Name: Digital Electronics **Subject Code: BTIC13304**

Type of course: PCC

Prerequisite (if any): Basic Electronics

List of Courses where this course will be prerequisite: Microcontroller and Interfacing, Digital Signal Processing, Image Processing

Rationale: This subject will help students to understand other subjects related to Digital Circuits, Computer Science, Telecommunication and VLSI. Students will be able to understand technologies used in electronic devices such as mobile phones, smart cards, digital computers etc.

Teaching and Examination Scheme:

TEACHING SCHEME				Theory Marks			Practical Marks		Total
L	T	P	C	TEE	CA1	CA2	TEP	CA3	
3	0	2	4	60	25	15	30	20	150

CA1: Continuous Assessment (assignments/projects/open book tests/closed book tests CA2: Sincerity in attending classes/class tests/ timely submissions of assignments/self-learning attitude/solving advanced problems TEE: Term End Examination TEP: Term End Practical Exam (Performance and viva on practical skills learned in course) CA3: Regular submission of Lab work/Quality of work submitted/Active participation in lab sessions/viva on practical skills learned in course

BSC: basic science course /ESC: Engineering Science Course /HSM: Humanities and management /PCC: Professional Core course /PEC: professional Elective course /OEC: Open Elective course/ MD: mandatory non-credit course

Content:

Sr. No.	Content	Total Hrs	
1	BINARY SYSTEM Digital computer and digital systems, Binary number, Number based conversion , Octal and Hexadecimal number, complements, binary codes, binary storage and register, binary logic , Integrated Circuit(IC)	**3**	**6 %**
2	BOOLEAN ALGEBRA AND LOGIC GATES Basic definition, axiomatic definition of Boolean algebra, basic theorems and properties of Boolean algebra, minterms and maxterms, logic operations, digital logic gates, universal gates	**4**	**9 %**
3	SIMPLIFICATION OF BOOLEAN FUNCTIONS K map method, two, three and four variable k map method, product of sum simplification, NAND or NOR implementation, don't care condition, tabulation method	**5**	**12 %**
4	COMBINATIONAL LOGIC Introduction, design procedure, adder, subtractor, code conversion	**3**	**6 %**
5	COMBINATIONAL LOGIC WITH MSI AND LSI Introduction, binary parallel adder, decimal adder, look ahead carry adder, excess-3 adder, binary multiplier, parity bit generator/checker, magnitude comparator, encoder, decoder, multiplexer, demultiplexer	**6**	**14 %**
6	SEQUENTIAL LOGIC Introduction, flip-flops, triggering of flip-flops, analysis of clocked sequential circuits, state reduction and assignment, flip flop excitation tables, design procedure, design of counters, design with state equations, finite state model, synthesis of synchronous	**8**	**18 %**

	sequential circuits, serial binary adder with Moore type FSM, the sequence detector, Mealy type model, Moore type circuit.		
7	REGISTERS AND COUNTERS Introduction, registers, shift registers, ripple counters, synchronous counters, timing sequences	**6**	**15 %**
8	DIGITAL LOGIC FAMILIES Introduction, characteristics of digital ICs, Resistor Transistor Logic(RTL),Diode Transistor Logic(DTL), Transistor Transistor Logic(TTL), Emitter Coupled Logic(ECL), Tri-state logic	**5**	**10 %**
9	REGISTERS TRANSFER LOGIC & MICRO OPERATION: Introduction, Inter-register Transfer, Arithmetic, logic and shift Micro- Operations, Conditional Control Statements, Fixed-Point Binary Data, overflow, Arithmetic Shifts, Decimal Data, Floating-Point Data, Instruction Codes, Design of Simple Computer.	**5**	**10 %**

Suggested Specification table with Marks (Theory):

% Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10 %	**20 %**	**20 %**	**10 %**	**20 %**	**20 %**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

Sr no	Title of book /article	Author(s)	Publisher and details like ISBN	Year of publication	Publication Edition
1	Digital Logic and Computer Design	M Morris Mano	Person, LPE,	2009	4th ed.
2	Fundamentals of Digital circuits	A. Anandkumar	PHI		2nd Ed
3	Principle of Digital Electronics	Malvino & Leach	McGraw-Hill	1975	2nded
4	Modern Digital Electronics	R.P.Jain	McGraw-Hill	2010	4th ed.
5	Digital Logic: Operation and Analysis	Boyce J. C	Prentice Hall	1982	2nded.

Course Outcomes: After completion of this course, students will be able to,

Sr. No.	CO statement	Marks % weightage
CO-1	apply knowledge of Boolean algebra and other minimization techniques to optimize logic circuit design	20
CO-2	examine the structure of various number systems and its application in digital design.	25
CO-3	identify, formulate and solve a problem based on combinational and sequential circuits such as decoders, encoders, multiplexers, de-	20

	multiplexers, flip-flops, counters, registers.	
CO-4	select the appropriate hardware and software tools for combinational and sequential circuit design.	20
CO-5	explain the different logic families involved in the digital system.	15

Mapping with POs:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO-1	3	0	0	0	0	0	0	0	0	0	0	0	2	1	0
CO-2	3	0	0	0	0	0	0	0	0	0	0	0	1	1	0
CO-3	3	2	1	0	0	0	0	0	1	0	0	1	3	1	0
CO-4	3	2	1	0	0	0	0	0	1	0	0	1	3	1	0
CO-5	3	2	1	0	0	0	0	0	1	0	0	1	3	1	0
Rationale*															

Rationale*: Explaining why it is matching this particular program outcome

List of Open learning website:

https://onlinecourses.nptel.ac.in/noc22_ee55/preview

List of Open Source Software:

Simulation Program with Integrated Circuit Emphasis(**spice), circuit logix**

FOR LAB SESSIONS:

List of Experiments:

1. Verification of logic gates using digital ICs
2. Configuring NAND and NOR gates as universal logic gates.
3. Implementation of Boolean Logic Functions using logic gates and combinational circuits
4. Measure digital logic gates specifications such as propagation delay, noise margin, Fan-in and Fan-out
5. Design and implementation of Binary Half adder and full adder,
6. Design and implementation of half subtractor, full subtractor and Parallel adder.
7. Design and implementation of code converters.
8. Design and implementation of Encoder and Decoder.
9. Design and implement of Magnitude comparator.
10. Design and implementation of multiplexer and de-multiplexer.
11. Design and Implement JK-flip-flop, RS-flip-flop, D – flip-flop and T-flip-flop using digital Ics.
12. Design and Implement JK-flip-flop and RS-flip-flop using logic gates.
13. Design and implement universal shift registers using digital IC.
14. Design and implement Asynchronous Counters.
15. Design and implement synchronous Counters.

Major Equipment Needed: Digital Storage Oscilloscope (DSO), CROs, Multi-meters, Function generator, Bread board trainer, Logic gate ICs